Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A system to test integrated circuits on a wafer, comprising:

a transceiver formed on the wafer, in an area other than an area used to form an integrated circuit; and

an antenna system couplable to the transceiver.

2. (Original) The system of claim 1, wherein the transceiver is couplable to a plurality of integrated circuits formed on the wafer to test selected ones of the plurality of integrated circuits.

3. (Original) The system of claim 2, wherein the transceiver is adapted to apply test signals to at least one selected integrated circuit of the plurality of integrated circuits to test the at least one selected integrated circuit in response to the antenna system receiving a signal.

4. (Original) The system of claim 2, wherein the antenna system is adapted to transmit signals corresponding to results from testing at least one selected integrated circuit of the plurality of integrated circuits.

5. (Original) The system of claim 2, further comprising a multiplexing circuit to couple the transceiver to each of the plurality of integrated circuits.

6. (Original) The system of claim 1, wherein the antenna system comprises one of a loop antenna, a pair of dipole antennas or an antenna array formed by loop or dipole antenna elements.

7. (Original) The system of claim 1, further comprising:

a plurality of transceivers, each adapted to receive and transmit signals to test selected ones of a multiplicity of integrated circuits formed on the wafer and each of the transceivers being formed at a different location on the wafer; and

a plurality of antenna systems, each antenna system being coupleable to at least one of the plurality of transceivers and each of the plurality of antenna systems being formed at different locations on the wafer.

8. (Original) The system of claim 7, wherein each transceiver of the plurality of transceivers or each transceiver in a subset of transceivers of the plurality of transceivers are each adapted to transmit test result signals simultaneously on different radio frequencies.

9. (Original) The system of claim 7, wherein each of the antenna systems is formed to minimize electromagnetic interference with the multiplicity of integrated circuits during testing.

10. (Original)The system of claim 7, wherein each of the transceivers and antenna systems are formed in a predetermined distribution on the wafer.

11. (Original) The system of claim 10, wherein the predetermined distribution is adapted to minimize space utilization, facilitate optimum testing of a selected number of integrated circuits simultaneously, and to minimize electromagnetic interference with the integrated circuits during testing and between different transceivers and associated antenna systems.

12. (Original) The system of claim 7, further comprising a multiplexing circuit, wherein an integrated circuit to be test and an associated transceiver are selectable by at least one of a word-line or a bit-line and wherein the transceiver is adapted to select a proper stream of test data of the integrated circuit under test from the multiplexing circuit.

13. (Original) The system of claim 7, further comprising a word-line/bit-line power distribution scheme adapted to select an integrated circuit to be tested and an associated transceiver and to distribute test mode power to the selected integrated circuit to be tested and the associated transceiver.

14. (Original) The system of claim 1, wherein the transceiver receives power via one of a probe, a radio frequency power signal, a word-line or a bit-line, and a pad electrically connectable to the transceiver, wherein the pad is connectable to an external power source.

15. (Original) The system of claim 1, further comprising a pad formed proximate to a periphery of the wafer and electrically connectable to the transceiver to provide power to the transceiver.

16. (Original) The system of claim 1, further comprising another transceiver and test unit external to the wafer and adapted to transmit scan test vectors to the transceiver on the wafer and to receive test results from the transceiver on the wafer.

17. (Original) The system of claim 16, wherein the transceiver is adapted to transmit self-test data and to receive and transmit scan test vectors from the external transceiver and test unit.

18. (Original) The system of claim 1, wherein the transceiver is adapted to provide one of an amplitude shift keying (ASK) or an on-off keying (OOK) modulation scheme.

19. (Original) The system of claim 1, wherein the transceiver is adapted to receive and to transmit signals to perform real-time tests periodically during fabrication of the wafer.

20. (Original) The system of claim 1, wherein the transceiver is adapted receive and to transmit signals to perform tests under burn-in stress conditions or other environmental extremes.

21. (Original) The system of claim 1, wherein the transceiver comprises:

a down converter to convert a received radio frequency (RF) signal to an intermediate frequency (IF) signal;

a received signal strength indicator (RSSI);

a limiting amplifier to amplify the IF signal in response to the RSSI; and

a comparator to generate a data signal in response to the amplified IF signal.

22. (Original) The system of claim 1, wherein the transceiver comprises:

a phase/frequency detector to receive an input or reference signal;

a charge pump to receive an output signal from the phase/frequency detector;

a filter to filter selected frequency band signals from a charge pump signal;

a voltage controlled oscillator to receive a filtered signal from the filter; and

a power amplifier to modulate a carrier signal from the voltage controlled oscillator by a data input signal.

23. (Currently Amended) The system of claim 1, wherein the transceiver is formed in one of a scribe line formed in the wafer~~, on a chip of each integrated circuit, on another chip on the wafer not used to form an integrated circuit,~~ or on an unusable portion of the wafer.

24. (Original) The system of claim 1, wherein the antenna system comprises an antenna system formed in at least one of a same scribe line as the transceiver, in at least one other scribe line formed in the wafer, on a chip on the wafer not used to form an integrated circuit or on an usable portion of the wafer.

25. (Original) The system of claim 24, wherein the antenna system comprises:

a loop antenna adapted to be shared by a plurality of transceivers; and

a plurality of differential amplifier circuits, each differential amplifier circuit being associated with one of the plurality of transceivers, wherein only one of the plurality of differential amplifier circuits is active at any given time to permit the associated transceiver to receive or transmit signals.

26. (Original) The system of claim 24, wherein the antenna system further comprises an inductor connected in parallel with each differential amplifier circuit, wherein the inductor completes the loop antenna when an associated differential amplifier circuit is disabled.

27. (Original) The system of claim 24, wherein the antenna system further comprises:

a pair of inductors connected in parallel with each differential amplifier circuit, wherein the pair of inductors complete the loop antenna when an associated differential amplifier circuit is disabled; and

a field effect transistor (FET) to couple a voltage source to a node between each pair of inductors, wherein the voltage source is connected to the node in response to an RF carrier signal from an associated one of the plurality of transceivers being applied to a gate of the FET.

28. (Original) The system of claim 1, wherein the antenna system comprises an antenna external to the wafer and wherein the transceiver is connectable to the antenna by a wafer boat or fixture.

29. (Original) The system of claim 1, further comprising:

an insulative layer formed on the wafer; and

a conductive layer formed on the insulative layer and electrically connecting to the transceiver via an opening formed in the insulative layer to test selected ones of the integrated circuits during manufacturing, wherein the insulative layer and the conductive layer are removable for further fabrication of the integrated circuits.

30. (Currently Amended) A system to test integrated circuits on a wafer, comprising:

a plurality of transceivers each adapted to receive and transmit signals to test selected ones of a multiplicity of integrated circuits formed on the wafer and each of the transceivers being formed at a different location on the wafer in one of a plurality of scribe lines formed in the wafer or at other locations on the wafer in areas other than areas used to form integrated circuits; and

at least one antenna systems couplable to the plurality of transceivers.

31. (Original) The system of claim 30, further comprising a multiplexing circuit to couple each transceiver selectively to one of a predetermined number of the multiplicity of integrated circuits.

32. (Original) The system of claim 30, wherein each transceiver of the plurality of transceivers or each transceiver in a subset of transceivers of the plurality of transceivers are each adapted to transmit signals corresponding to test results simultaneously on different radio frequencies.

33. (Original) The system of claim 30, wherein each of the transceivers and associated antenna systems are formed in a predetermined distribution on the wafer.

34. (Original) The system of claim 30, further comprising a word-line/bit-line distribution scheme adapted to select each integrated circuit to be tested and an associated transceiver.

35. (Original) The system of claim 30, wherein each transceiver is powered via one of a probe, a radio frequency power signal, a word-line/bit-line power distribution scheme and a pad electrically connectable to the transceiver, wherein the pad is connectable to an external power source.

36. (Original) The system of claim 30, wherein each transceiver comprises:

a down converter to convert a received radio frequency (RF) signal to an intermediate signal (IF);

a received signal strength indicator (RSSI);

an amplifier to amplify the IF signal in response to the RSSI; and

a comparator to generate a data signal in response to the amplified IF signal.

37. (Original) The system of claim 30, wherein each transceiver comprises:

a phase/frequency detector to receive an input or reference signal;

a charge pump to receive an output signal from the phase/frequency detector;

a filter to filter signals in a selected frequency band from the charge pump;

a voltage controlled oscillator to receive a filtered signal from the filter; and

a power amplifier to modulate a carrier signal from the voltage controlled oscillator by a data signal.

38. (Original) The system of claim 30, wherein the at least one antenna system comprises an antenna external to the wafer and wherein each of the plurality of transceivers is connectable to the antenna by a wafer boat or fixture.

39. (Original) The system of claim 30, further comprising a plurality of antenna systems, each antenna system being coupleable to at least one of the plurality of transceivers and each of the plurality of antenna systems being formed at different locations on the wafer in at least one of the plurality of scribe lines.

40. (Original)The system of claim 39, wherein each antenna system comprises one of a loop antenna, a pair of dipole antennas or an antenna array formed by loop or dipole antenna elements.

41. (Original) The system of claim 39, wherein each antenna system comprises:

a loop antenna adapted to be shared by a predetermined number of the plurality of transceivers; and

a plurality of differential amplifiers, each differential amplifier being associated with one of the predetermined number of transceivers, wherein only one of the plurality of differential amplifiers is active at any given time to permit the associated transceiver to receive or transmit signals.

42. (Original) The system of claim 30, further comprising:

an insulative layer formed on the wafer; and

a conductive layer formed on the insulative layer in line traces electrically connecting to each of the plurality of transceivers via openings formed in the insulative layer to test selected ones of the integrated circuits during manufacturing, wherein the insulative layer and the conductive layer are removable for further fabrication of the integrated circuits.

43. (Original)A transceiver to test integrated circuits on a wafer, comprising:

a down converter to convert a received radio frequency (RF) signal to an intermediate frequency (IF) signal;

a received signal strength indicator (RSSI);

an amplifier to amplify the IF signal in response to the RSSI; and

a comparator to generate a data signal in response to the amplified IF signal.

44. (Original) The transceiver of claim 43, wherein each of the down converter, RSSI, amplifier and comparator are formed in a scribe line formed in the wafer.

45. (Original) The transceiver of claim 43, further comprising:

a phase/frequency detector to receive an input or reference signal;

a charge pump to receive an output signal from the phase/frequency detector;

a filter to filter signals in a selected frequency band from the charge pump;

a voltage controlled oscillator to receive a filtered signal from the filter; and

a power amplifier to modulate a carrier signal from the voltage controlled oscillator.

46. (Original) The transceiver of claim 45, wherein each of the phase/frequency detector, charge pump, filter, voltage controlled oscillator and power amplifier are formed in a scribe line formed in the wafer.

47. (Original) An antenna system to test integrated circuits on a wafer, comprising:

a loop antenna adapted to be shared by a plurality of transceivers; and

a plurality of differential amplifier circuits, each differential amplifier circuit being associated with one of the plurality of transceivers, wherein only one of the plurality of differential amplifier circuits is active at any given time to permit the associated transceiver to receive or transmit signals.

48. (Original) The antenna system of claim 47, wherein each of the loop antenna and the plurality of differential amplifier circuits are formed in at least one scribe line formed in the wafer.

49. (Original) The antenna system of claim 47, wherein the antenna system further comprises at least one inductor connected in parallel with each differential amplifier circuit, wherein the at least one inductor completes the loop antenna when an associated differential amplifier circuit is disabled.

50. (Original) The antenna system of claim 47, further comprising:

a pair of inductors connected in parallel with each differential amplifier circuit, wherein the pair of inductors complete the loop antenna when an associated differential amplifier circuit is disabled; and

a field effect transistor (FET) to couple a voltage source to a node between each pair of inductors, wherein the voltage source is connected to the node in response to an RF carrier signal from an associated one of the plurality of transceivers being applied to a gate of the FET.

51. (Original) The antenna system of claim 47, wherein the loop antenna is physically small compared to a wavelength at which the loop antenna operates.

52. (Currently Amended) A method of making a system to test integrated circuits on a wafer, comprising:

forming a transceiver on the wafer, wherein the transceiver is formed in an area other than an area used to form an integrated circuit; and

providing an antenna system couplable to the transceiver.

53. (Currently Amended) The method of claim 52, wherein forming the transceiver comprises forming the transceiver in one of a scribe line~~, on a chip~~ or on an unusable portion of the wafer.

54. (Original) The method of claim 52, further comprising forming a multiplexing circuit to couple the transceiver to each of a plurality of integrated circuits.

55. (Original) The method of claim 52, further comprising:

forming a plurality of transceivers, each adapted to receive and transmit signals to test selected ones of a multiplicity of integrated circuits formed on the wafer and each of the transceivers being formed at different location on the wafer in one of a plurality of scribe lines formed in the wafer; and

forming a plurality of antenna systems, each antenna system being coupleable to at least one of a plurality of transceivers and each of the plurality of antennas systems being formed at different locations on the wafer in at least one of a plurality of scribe lines.

56. (Original) The method of claim 55, further comprising forming each of the transceivers and associated antenna systems in a predetermined distribution on the wafer.

57. (Original) The method of claim 55, wherein forming each transceiver comprises:

forming a down converter to convert a received radio frequency (RF) signal to an intermediate (IF) signal;

forming a received signal strength indicator (RSSI);

forming an amplifier to amplify the IF signal in response to the RSSI; and

forming a comparator to generate a data signal in response to the amplified IF signal.

58. (Original) The method of claim 55, wherein forming each transceiver comprises:

forming a phase/frequency detector to receive an input or reference signal;

forming a charge pump to receive an output signal from the phase/frequency detector;

forming a filter to filter signals in a selected frequency band from the charge pump;

forming a voltage controlled oscillator to receive a filtered signal from the filter; and

forming a power amplifier to modulate a carrier signal from the voltage controlled oscillator by a data signal.

59. (Original) The method of claim 55, wherein forming each antenna system comprises forming one of a loop antenna, a pair of dipole antennas or an antenna array formed by loop or dipole antenna elements.

60. (Original) The method of claim 55, wherein forming each antenna system comprises:

forming a loop antenna adapted to be shared by a predetermined number of the plurality of transceivers; and

forming a plurality of differential amplifier circuits, each differential amplifier circuit being associated with one of the predetermined number of transceivers, wherein only one of the plurality of differential amplifier circuits is active at any given time to permit the associated transceiver to receive or transmit signals.

61. (Currently Amended) A method to test integrated circuits on a wafer, comprising:

selecting at least one integrated circuit of a plurality of integrated circuits to be tested;

performing a test or self-test on the at least one selected integrated circuit in response to selecting the at least one integrated circuit; and

transmitting test results via a transceiver associated with the at least one selected integrated circuit, wherein the transceiver is formed on the wafer in an area other than an area used to form one of the plurality of integrated circuits.

62. (Original) The method of claim 61, wherein selecting the at least one integrated circuit comprises using a word-line/bit-line distribution.

63. (Original) The method of claim 61, further comprising transmitting test results of the at least one selected integrated circuit to an external transceiver.

64. (Original)The method of claim 61, wherein transmitting the test results comprises transmitting in one of an amplitude shift keying (ASK) or an on-off keying (OOK) modulation scheme.

65. (Currently Amended) The method of claim 61, wherein the transceiver is formed in one of a scribe line in the wafer~~, on a chip~~ or on an unusable portion of the wafer.

66. (Original) The method of claim 61, further comprising applying power to the at least one selected integrated circuit via one of a probe, radio frequency power signal, a pad electrically connectable to an external power source, a word-line or a bit-line.

67. (Original) The method of claim 61, further comprising applying power to the transceiver associated with the at least one selected integrated circuit via one of a probe, radio frequency power signal, a pad electrically connectable to an external power source, a word-line or a bit-line.

68. (Original) The method of claim 61, further comprising receiving and transmitting signals to perform real-time tests of the at least one selected integrated circuit during at least one of fabrication and burn-in of the wafer.

69. (Original) The method of claim 61, further comprising transmitting an RF signal to a transceiver associated with the at least one selected integrated circuit to test the integrated circuit.

70. (Original) The method of claim 61, further comprising:

forming an insulative layer on the wafer; and

forming a conductive layer on the insulative layer in line traces electrically connecting to each of a plurality of transceivers via openings formed in the insulative layer to test selected ones of the integrated circuits during manufacturing; and

removing the insulative layer and the conductive layer for further fabrication of the integrated circuits.